	Microprocessor and Interfacing (CE and IT 4th Semester) **Unit 1: Introduction to microprocessor**
1	Which of the following is correct for microprocessor Intel 8085? a) **8 bit microprocessor** b) 16 bit microprocessor c) 4 bit microprocessor d) 32 bit microprocessor
2	MOS stands for _____ a) Material Operating Semiconductor b) **Metal Oxide Semiconductor** c) Metal Operating Segment d) None of the mentioned
3	Which of the following part of the microprocessor is close related to register? a) Processor b) CPU c) ALU d) **Memory**
4	Which of the following is not a special function register? a) Program counter b) Instruction pointer c) **Accumulator** d) Stack pointer
5	SP stands for _____ a) **Stack pointer** b) Segment pointer c) Status pointer d) State pointer
6	Which of the following is not a valid instruction type? a) Zero operant b) Single operand c) Two operand d) **None of the mentioned**
7	The ROM programmed during manufacturing process itself is called a. **MROM** b. PROM c. EPROM d. EEPROM
8	A field programmable ROM is called a. MROM b. **PROM** c. FROM d. FPROM
9	**The first micro-processor had a (n) _____.** a) 1-bit data bus b) 2- bit data bus c) 3-bit data bus **d) 4-bit data bus**

10	**_____ Processor is first introduced by the Intel in 1971.** a) 8080 b) 4004 c) 8008 d) 8085
11	Which of the following is/are 8-bit micro processor? a) 8008 b) 8080 c) 8085 d) **All of the mentioned**
12	The limitations of the 8-bit microprocessors was/were is _____. a) Low speed of execution b) Low memory addressing capability c) Less powerful instruction set d) **All of the mentioned**
13	Intel's 8086 were launched in the year_____. a) 1971 b) 1972 c) 1974 d) **1978**
14	Which is the microprocessor comprises? a) Register section b) One or more ALU c) Control unit d) **All of the mentioned**
15	If SRAM (Static RAM)has . In which of the following modes this SRAM is operating **A.** Read **B. Write** **C.** Stand by **D.** none of the above
16	Which of the following is true with respect to EEPROM(Electrically Erasable Programmable ROM)? • **A.** Contents can be erased byte wise only

	• **B.** Contents of full memory can be erased together • **C. Contents can be erased using Ultra Violet Rays** • **D.** Contents cannot be erased
17	Full form of SD RAM? • **A. Synchronous Dynamic RAM** • **B.** Static Dynamic RAM • **C.** Semi Dynamic RAM • **D.** Second Dynamic RAM
18	Which of the following is present In 8088 Micro processor • **A.** 16 bit data bus • **B.** 4 byte pre – fetch queue • **C.** 6 byte pre – fetch queue • **D. 16 bit address bus**
19	8085 microprocessor is a ____ device • **A.** PMOS • **B.** CMOS • **C. NMOS** • **D.** QMOS
20	The input and output operations are respectively similar to the operations, a) read, read b) write, write c) **read, write** d) write, read
21	A central processing unit, fabricated on a single chip of semiconductor is called: **a. Microprocessor** b. RAM c. ROM d. None of these
22	Which is the architecture of microprocessor: a. CISC b. RISC **c. All of these** d. None of these
23	CISC stands for: a. Complex Instruction System Computer b. Complex Instruction Set Car **c. Complex Instruction Set Computer** d. None of these
24	Which is the components of computer: a. System Bus b. CPU c. Memory Unit **d. All of these**
25	System Bus Contains: a. Address Bus b. Data Bus c. Control Bus

	d. All of these
26	Microprocessor is the _____ of computer: a. Hand b. Heart **c. Brain** d. Leg
27	Microprocessor is fabricated on single chip using: **a. MOS** b. ALU c. CPU d. All of these
28	Which is the components of microprocessor: a. Register unit b. Arithmetic and logical unit c. Timing and control unit **d. All of these**
29	Which is an integral part of any microcomputer system and its primary purpose is to hold program and data: **a. Memory unit** b. Register unit c. A and B d. None of these
30	Which system communicates with the outside word via the I/O devices interfaced to it: a. Microprocessor **b. Microcomputer** c. Digital computer d. All of these
31	A computer which has the microprocessor as_____ is called as a microcomputer: **a. CPU** b. ALU c. RU d. None of these
32	The___ was very successful in the calculator market at that time: a. Motorola 6800 and 6809 **b. Microprocessor 4004** c. Intel 8085 d. None of these
33	Which Microprocessor producer continue successfully to create newer and improved version of the microprocessor: a. Intel b. Motorola **c. Both A and B** d. None of these
34	How many bit microprocessor developed by Intel: a. 4 bit **b. 8 bit** c. 32 bit d. 64 bit
35	Which is the main feature of 8085:

	a. Internal clock generator b. Internal system controller c. Higher clock frequency **d. All of these**
36	PC's use____ based on this architecture: **a. CPU** b. ALU c. MU d. None of these
37	What is the store by register: **a. data** b. operands c. memory d. None of these
38	In Microprocessor one of the operands holds a special register called: a. Calculator b. Dedicated **c. Accumulator** d. None of these
39	A set of register which contain are: a. data b. memory addresses c. result **d. all of these**
40	PC stands for: **a. Program counter** b. Points counter c. Paragraph counter d. Paint counter
41	SP stands for: a. Status pointer **b. Stack pointer** c. a and b d. None of these
42	A nibble can be represented in the form of: a. Octal digit b. Decimal **c. Hexadecimal** d. None of these
43	MSD stands for: a. Least significant digit **b. Most significant digit** c. Medium significant digit d. low significant digit
44	CPU can read & write data by using : a. Control bus **b. Data bus** c. Address bus d. None of these

45	Which bus transfer singles from the CPU to external device and others that carry singles from external device to the CPU: **a. Control bus** b. Data bus c. Address bus d. None of these
46	The ram which is created using bipolar transistors is called: a. Dynamic RAM **b. Static RAM** c. Permanent RAM d. DDR RAM
47	Which type of RAM needs regular referred: **a. Dynamic RAM** b. Static RAM c. Permanent RAM d. SD RAM
48	The ____ place the data from a register onto the data bus: **a. CPU** b. ALU c. Both A and B d. None of these
49	The CPU sends out a ____ signal to indicate that valid data is available on the data bus: a. Read **b. Write** c. Both A and B d. None of these
50	How many bit stored by status register: **a. 1 bit** b. 4 bit c. 6 bit d. 8 bit

	Unit 2: The 8085 microprocessor architecture
1	How many flags does 8085 have? a) 4 b) **5** c) 8 d) 9
2	Which of the following is used for storing flag registers? **Status register** Control register Buffer register None of the mentioned
3	Which of the following function relate to stack? a) **Push and pop** b) Call and return c) Both push pop and call return d) None of the mentioned

4	Program counter in a digital computer a. Counts the numbers of programs run in the machine. b. Counts the number of times a subroutine is called. c. Counts the number of times the loops are executed. d. **Points the memory address of the next instruction to be fetched.**
5	At the beginning of a fetch cycle, the contents of the program counter are a. incremented by one. b. transferred to address bus. c. **transferred to memory address register.** d. transferred to memory data register.
6	The number of address and data lines of 8085 are____. a) 8 and 8 b) **16 and 8** c) 8 and 16 d) 16 and 16
7	A 16-bits address bus can generate _____addresses. a) 32767 b) 25652 c) **65536** d) None of the mentioned
8	If there is a carry from lowest nibble during addition, _____ flag sets. a) Carry b) **Auxiliary carry** c) Over flow d) Sign
9	Which is not part of execution unit? a) ALU b) **Address conversion mechanism** c) Flag register d) General purpose registers
10	If the size of the segment is 64 kb, what will be the starting and ending off set addresses of it a) 0000H to 7FFFH b) **0000H to FFFFH** c) 8000H to FFFFH

	d) 00000H to FFFFFH
11	Which of the following is the 16bit registors in 8085 processor **A.** Stack Pointer **B.** Program Counter **C.** IR **D. a and b**
12	Which of the following depends on the microprocessor speed **A.** Clock **B.** Data Bus Width **C. Address Bus Width** **D.** Size of Register
13	Which of the following pins are used in the microprocessor to request & acknowledge a DMA Transfer (Direct Memory Access) • **A.** Ready & Wait • **B.** Reset & Ready • **C. Hold & HLDA** • **D.** None of these
14	_____ number of address lines required to address a memory of size 32 K • **A.** 14 lines • **B. 15 lines** • **C.** 16 lines • **D.** 18 lines
15	Which of the following register deals with sequencing the execution of instructions • **A.** Stack Pointer • **B. Program Counter** • **C.** Accumulator • **D.** Flag
16	In Stack , data storage is designed in _____ method • **A.** First in first out • **B.** last in last out • **C. last in first out** • D. first in last out
17	Which of the following is an 8085 hardware interrupt • **A.** TRAP • **B.** RST 6.5 • **C.** RST 7.5 • **D. All the above**
18	Which of the following flag register doesn't belong to 8085 • **A.** Carry flag • **B.** Sign flag • **C.** Zero flag • **D. One flag**
19	1GB is equal to _____ • **A.** 1 billion bytes • **B.** 1000 KB • **C. 1000 MB** • **D.** 1024 bytes
20	Which of the following are the two power connections for +5 volts in 8085

	• **A.** Vss & Vgg • **B. Vcc & Vss** • **C.** Vcc & Vgg • **D.** None of these
21	The operation, IOWR (active low) performs a) write operation on input data b) **write operation on output data** c) read operation on input data d) read operation on output data
22	In memory-mapped scheme, the devices are viewed as a) distinct I/O devices b) **memory locations** c) only input devices d) only output devices
23	The act of acquiring an instruction is referred as the____ the instruction: **a. Fetching** b. Fetch cycle c. Both a and b d. None of these
24	The area of memory with addresses near zero are called: a. High memory b. Mid memory c. Memory **d. Low memory**
25	Stack words on: a. LILO **b. LIFO** c. FIFO d. None of these
26	Which pin provides a reset out option in 8085? a) Pin 1 **b) Pin 3** c) Pin 11 d) Pin 9
27	_____ a subsystem that transfer data between computer components inside a computer or between computer: a. Chip b. Register c. Processor **d. Bus**
28	Which bus carry addresses: a. System bus **b. Address bus** c. Control bus d. Data bus
29	A 16 bit address bus can generate___ addresses: a. 32767 b. 25652 **c. 65536** d. none of these

30	Which technique is used for main memory array design: a. Linear decoding b. Fully decoding **c. Both A and B** d. None of these
31	CS stands for: a. Cable select **b. Chip select** c. Control select d. Cable system
32	The capacity of this chip is 1KB they are organized in the form of 1024 words with 8 bit word The what is the site of address bus: a. 8 bit **b. 10 bit** c. 12 bit d. 16 bit
33	The collection of the above mentioned entities where data is stored is called _____ a) Block b) Set **c) Word** d) Byte
34	WE stands for: **a. Write enable** b. Wrote enable c. Write envy d. None of these
35	A___ on this pin indicates a memory operation: **a. Low** b. High c. Medium d. None of these
36	The external device is connected to a pin called the _____ pin on the processor chip. **a. Interrupt** b. Transfer c. Both d. None of these
37	Eight of the register are known as: **a. General- purpose register** b. Pointer or index registers c. Segment registers d. Other register
38	ALE stand for: **a. Address latch enable** b. Address light enable c. Address lower enable d. Address last enable
39	Which causes the microprocessor to immediately terminate its present activity: **a. RESET signal**

	b. INTERUPT signal c. Both d. None of these
40	INTR: it implies the_____ signal: **a. INTRRUPT REQUEST** b. INTRRUPT RIGHT c. INTRRUPT RONGH d. INTRRUPT RESET
41	INTA stands for: **a. Interrupt acknowledge** b. Interrupt access c. Interrupt address d. None of these
42	Who is the determined by the time taken by the stages the requires the most processing time: **a. Clock period** b. Flow through c. Throughput d. None of these
43	Which pin provides an ALE option in 8085? a) Pin 13 b) Pin 11 c) Pin 30 d) Pin 8
44	Ready pin of microprocessor is used a. to indicate that microprocessor is ready to receive inputs b. to indicate that microprocessor is ready to receive outputs **c. to introduce wait state** d. to provide direct memory access
45	A high on RESET OUT signifies that a. all the registers of the CPU are being reset b. all the registers and counters are being reset c. **all the registers and counters are being reset and this signal can be used to reset external support chip** d. processing can begin when this signal goes high
46	Which mnemonics is not valid in 8085 interrupt? a. RST 6.5 b. RST 7.5 c. RST 5.5 d. **READY**
47	The continuous transfer may be interrupted by an external device by pulling down the signal a. HRQ b. DACK (active low) c. DACK (active high) **d. HLDA**
48	Which pin is used to demultiple address bus and data bus? a) READY **b) ALE** c) HLDA

	d) HOLD
49	Which storage technique dose not decoding circuit: **a. Linear decoding** b. Fully decoding c. Partially d. None of these
50	Which pin provide VCC and VSS options in 8085? a) Pin 10 and 20 b) Pin 20 and 30 c) Pin 30 and 10 d) **Pin 40 and 20**

	Unit 3: The 8085 memory interfacing
1	HLT opcode means a. load data to accumulator b. store result in memory c. load accumulator with contents of register d. **end of program**
2	Which one of the following addressing mode is not possible in 8085 • **A. Indexed addressing** • **B.** Indirect addressing • **C.** Direct addressing • **D.** Indirect register address
3	If the result of the arithmetic operation is zero then zero flag is set to _____ • **A. 1** • **B.** 0 • **C.** -1 • **D.** 2
4	_____ Stores the instruction currently being executed: **a. Instruction register** b. Current register c. Both a and b d. None of these
5	The subprogram finish the return instruction recovers the return address from the: a. Queue **b. Stack** c. Program counter d. Pointer
6	The four index register can be used for: **a. Arithmetic operation** b. Multipulation operation

	c. Subtraction operation d. All of these
7	_____ converts the programs written in assembly language into machine instructions. a) Machine compiler b) Interpreter **c) Assembler** d) Converter
8	The instructions like MOV or ADD are called as _____ a) OP-Code b) Operators c) Commands d) None of the mentioned
9	The purpose of the ORIGIN directive is _____ a) **To indicate the starting position in memory, where the program block is to be stored** b) To indicate the starting of the computation code c) To indicate the purpose of the code d) To list the locations of all the registers used
10	The condition flag Z is set to 1 to indicate _____ a) The operation has resulted in an error b) The operation requires an interrupt call **c) The result is zero** d) There is no empty register available
11	Assembly language programs are written using a) Hex Code **b) Mnemonics** c) ASCII Code d) None of these views
12	How many memory location are required to store the instruction LXI H, 0200H in 8085? a) 1 b) 2 **c) 3** d) 4
13	Programming language in which there is a very strong correspondence between the language and the architecture's machine code instructions is termed as A. machine language **B. assembly language** C. high level language D. medium language
14	CPU has built-in ability to execute a particular set of machine instructions, called as _____ **a) Instruction Set** b) Registers c) Sequence Set d) User instructions
15	The length of a register is called _____ a) word limit **b) word size**

	c) register limit d) register size
16	Which of the following is a data transfer instruction? **a) STA 16-bit address** b) ADD A, B c) MUL C, D d) RET
17	What is correct instruction if you want the control to go to the location 2000h? a) MOV 2000h b) MOV A, 2000h **c) JMP 2000h** d) RET 2000h
18	Which of the following is an arithmetic instruction? a) STA 16-bit address b) **ADD B** c) MOV C, D d) RET
19	The instruction DCR R inform the assemble to **a) decrement the content of R** b) decrement the data address by 1 c) convert the sign decimal number to binary d) none of the above
20	Which instruction is required to rotate the content of accumulator one bit right along with carry? a. RLC b. RAL c. RRC **d. RAR**
21	How many memory location are required to store the instruction LXI H, 0200H in 8085? a) 1 **b) 2** c) 3 d) 4
22	Which instruction is required to rotate the content of accumulator one bit left along with carry? a. RLC **b. RAL** c. RRC d. RAR
23	Instruction MOV C,A requires: **a) 1 byte** b) 2 byte c) 3 byte d) None of the above
24	Branch instruction 'JUMP IF ZERO' is an example of a. transferring branch **b. conditional branch** c. unconditional branch d. arithmetic branch

25	Which is the logical instruction in following a) ADD R b) SUB R **c) ANL R** d) DCR R
26	1 byte= ? a) 8 bits b) 4 bits c) 6 bits d) 10 bits
27	Which instruction is used to return from subroutine program in 8085 a) NOP **b) RET** c) HLT d) CALL
28	What is the function of XRL instruction? a) Logical AND operation b) Logical OR operation **c) Logical XOR operation** d) None of above
29	What is the function of SUB R instruction? a) Subtract the data from R to accumulator **b) Subtract the data from accumulator to R** c) Both a and b d) None of above
30	Which is the data transfer instruction in following a) ADD R b) SUB R c) ANL R **d) DCR R**
31	How many memory location are required to store the instruction ADD B in 8085? **a) 1** b) 2 c) 3 d) 4
32	The instruction INR R inform the assemble to a) Increment the data address by 1 **b) Increment the content of R** c) convert the sign decimal number to binary d) none of the above
33	Which instruction is required to rotate the content of accumulator one bit right without carry? a. RLC b. RAL **c. RRC** d. RAR
34	Instruction STA 6000H requires: a) 1 byte b) 2 byte

	c) 3 byte d) None of the above
35	The number of instructions actually executed by the microprocessor depends on the a) stack **b) loop count** c) program counter d) time duration
36	In case of subroutines, the actual number of instructions executed by the processor depends on a) loop count b) length of interrupt service routine **c) length of procedure** d) none
37	The logical instruction that affect the carry flag during its execution is a. XRL A; b. ANL A; c. ORL A; **d. RLC A;**
38	Instruction MVI B,20H requires: a) 1 byte **b) 2 byte** c) 3 byte d) None of the above
39	Which instruction is required to rotate the content of accumulator one bit left without carry? **a. RLC** b. RAL c. RRC d. RAR
40	Branch instruction 'JUMP IF CARRY' is an example of a. transferring branch **b. conditional branch** c. unconditional branch d. arithmetic branch
41	Which is the arithmetic instruction in following a) JMP 16bit **b) SUB R** c) ANL R d) DCR R
42	2 byte= ? a) 8 bits b) 4 bits **c) 16 bits** d) 10 bits
43	Which instruction is used to copy data from one location to other location in 8085 a) MVI A, 8 bit **b) MOV A,R** c) ADD R d) JMP 16 bit

44	Instruction CALL 2050H requires: e) 1 byte f) 2 byte **g) 3 byte** h) None of the above
45	The instruction CMP to compare source and destination operands it performs a. addition **b. subtraction** c. division d. multiplication
46	In instruction MVI A,23H; the 23H called as _____ a) OP-Code b) Commands **c) Operand** d) None of the mentioned
47	Which instruction is used to end the program in 8085 a) NOP b) RET **c) HLT** d) CALL
48	Which instruction is used to 'do nothing' the program in 8085 **a) NOP** b) RET c) HLT d) CALL
49	The task to be performed is called a) Commands **b) OP-Code** c) Operand d) None of the mentioned
50	Branch instruction 'JUMP' is an example of a. transferring branch b. conditional branch c. **unconditional branch** d. arithmetic branch